FAIRCHILD SEMICONDUCTOR TM

July 2000

FDC6327C

Dual N & P-Channel 2.5V Specified PowerTrench™ MOSFET

General Description

These N & P-Channel 2.5V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

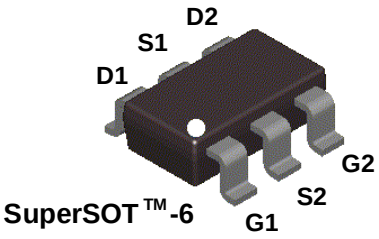
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

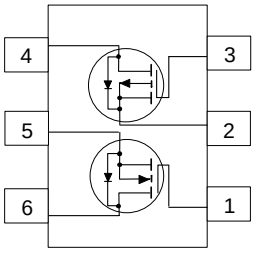
Applications

- DC/DC converter
- Load switch
- Motor driving

Features

- N-Channel 2.7A, 20V. $R_{DS(on)}$ = 0.08Ω @ V_{GS} = 4.5V
  $R_{DS(on)}$ = 0.12Ω @ V_{GS} = 2.5V
- P-Channel -1.6A, -20V. $R_{DS(on)}$ = 0.17Ω @ V_{GS} = -4.5V
  $R_{DS(on)}$ = 0.25Ω @ V_{GS} = -2.5V
- Fast switching speed.
- Low gate charge.
- High performance trench technology for extremely low $R_{DS(ON)}$.
- SuperSOT™-6 package: small footprint (72% smaller than SO-8); low profile (1mm thick).





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		20	-20	V
V_{GSS}	Gate-Source Voltage		±8	±8	V
I_D	Drain Current - Continuous	(Note 1a)	2.7	-1.9	A
	- Pulsed		8	-8	
P_D	Power Dissipation	(Note 1a)	0.96		W
		(Note 1b)	0.9		
		(Note 1c)	0.7		
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.327	FDC6327C	7”	8mm	3000

Electrical Characteristics

T_A = 25°C unless otherwise noted

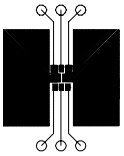
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA V_{GS} = 0 V, I_D = - 250 μA	N-Ch P-Ch	20 -20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C I_D = - 250 μA, Referenced to 25°C	N-Ch P-Ch		12 -19		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V V_{DS} = -16 V, V_{GS} = 0 V	N-Ch P-Ch			1 -1	μA
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V	All			-100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA V_{DS} = V_{GS}, I_D = -250 μA	N-Ch P-Ch	0.4 -0.4	0.9 -0.9	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C I_D = - 250 μA, Referenced to 25°C	N-Ch P-Ch		-2.1 2.3		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 2.7 A V_{GS} = 4.5 V, I_D = 2.7 A, T_J = 125°C V_{GS} = 2.5 V, I_D = 2.2 A V_{GS} = -4.5 V, I_D = -1.6 A V_{GS} = -4.5 V, I_D = -1.6 A, T_J = 125°C V_{GS} = -2.5 V, I_D = -1.3 A	N-Ch N-Ch N-Ch P-Ch P-Ch P-Ch		0.069 0.094 0.093 0.141 0.203 0.205	0.08 0.13 0.12 0.17 0.27 0.25	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V V_{GS} = -4.5 V, V_{DS} = -5 V	N-Ch P-Ch	8 -8			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 2.7 A V_{DS} = -5 V, I_D = -1.9 A	N-Ch P-Ch		7.7 4.5		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch P-Ch		325 315		pF
C_{oss}	Output Capacitance	P-Channel	N-Ch P-Ch		75 65		pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch P-Ch		35 24		pF

Electrical Characteristics (continued) T_A = 25°C unless otherwise noted

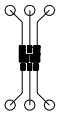
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A,	N-Ch P-Ch		5 7	15 14	ns
t_r	Turn-On Rise Time	V_{GS} = 4.5V, R_{GEN} = 6 Ω	N-Ch P-Ch		9 14	18 25	ns
$t_{d(off)}$	Turn-Off Delay Time	P-Channel V_{DD} = -10 V, I_D = -1 A,	N-Ch P-Ch		12 14	22 25	ns
t_f	Turn-Off Fall Time	V_{GS} = -4.5 V, R_{GEN} = 6 Ω	N-Ch P-Ch		3 3	9 9	ns
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 2.7 A, V_{GS} = 4.5V	N-Ch P-Ch		3.25 2.85	4.5 4.0	nC
Q_{gs}	Gate-Source Charge	P-Channel	N-Ch P-Ch		0.65 0.68		nC
Q_{gd}	Gate-Drain Charge	V_{DS} = -10 V, I_D = -1.9 A, V_{GS} = -4.5V	N-Ch P-Ch		0.90 0.65		nC
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch P-Ch			0.8 -0.8	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.8 A (Note 2) V_{GS} = 0 V, I_S = - 0.8 A (Note 2)	N-Ch P-Ch		0.76 -0.79	1.2 -1.2	V

Notes:

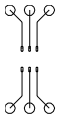
1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally.



a) 130 °C/W when mounted on a 0.125 in² pad of 2 oz. copper.



b) 140 °C/W when mounted on a 0.005 in² pad of 2 oz. copper.



c) 180 °C/W when mounted on a 0.0015 in² pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Typical Characteristics: N-Channel

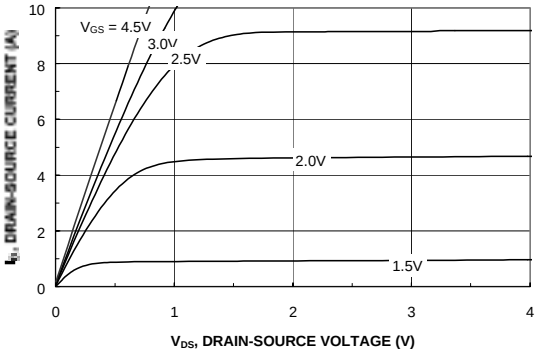


Figure 1. On-Region Characteristics.

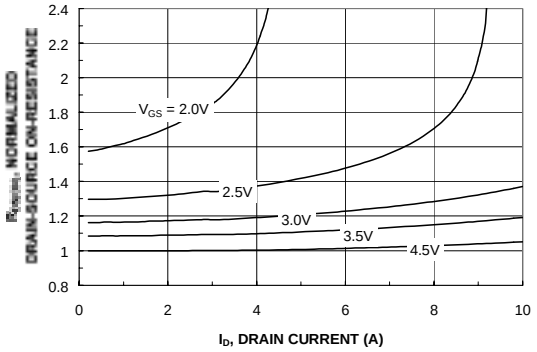


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

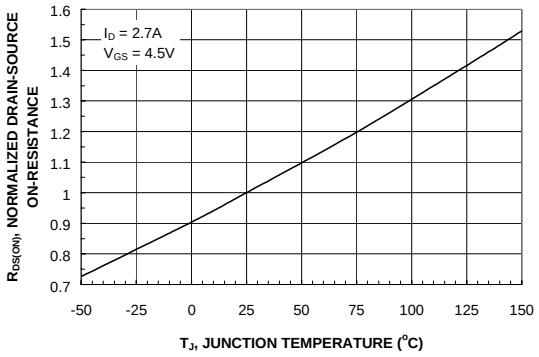


Figure 3. On-Resistance Variation with Temperature.

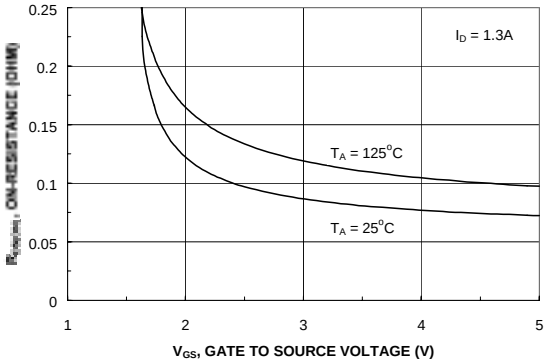


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

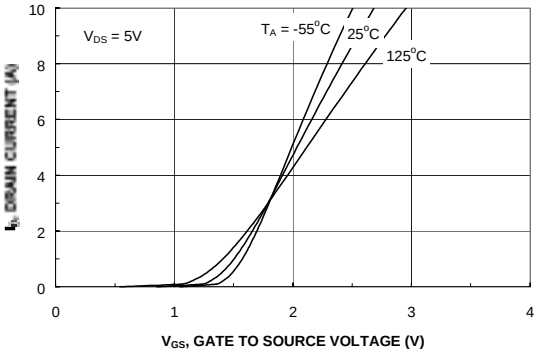


Figure 5. Transfer Characteristics.

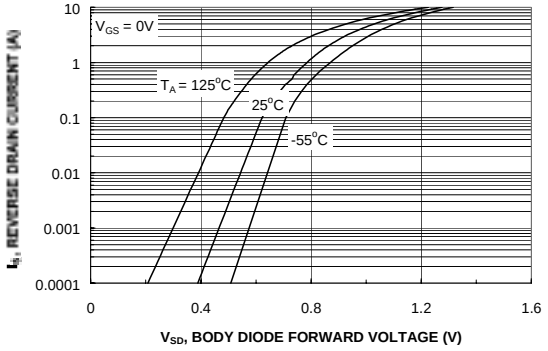


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-Channel (continued)

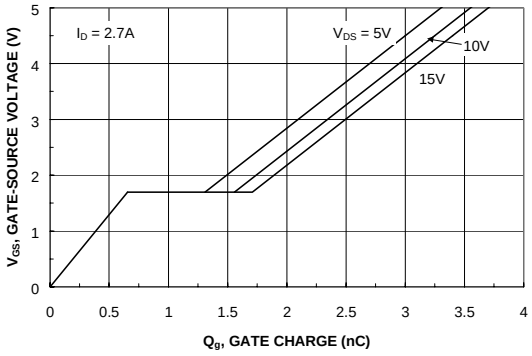


Figure 7. Gate-Charge Characteristics.

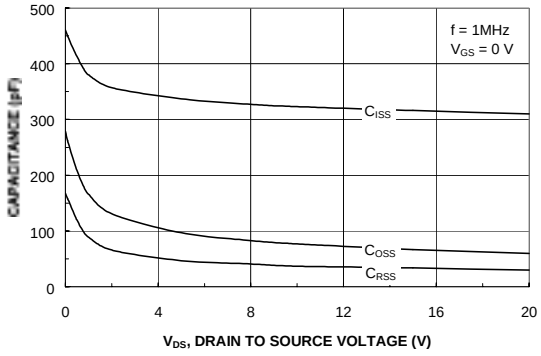


Figure 8. Capacitance Characteristics.

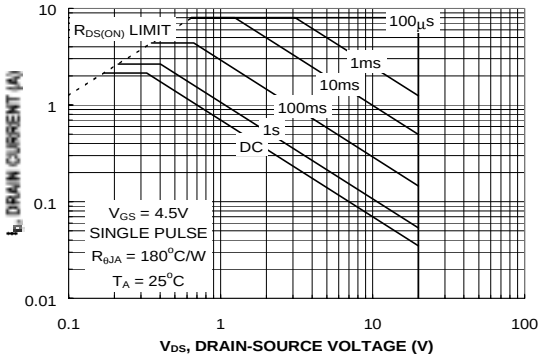


Figure 9. Maximum Safe Operating Area.

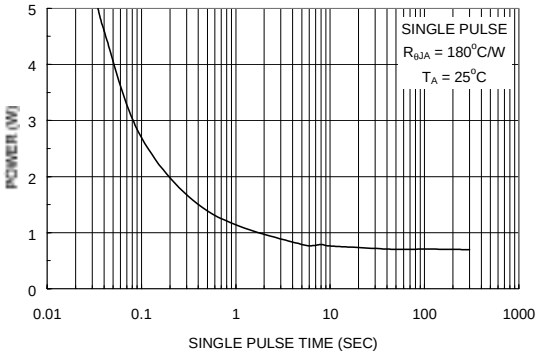


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: P-Channel

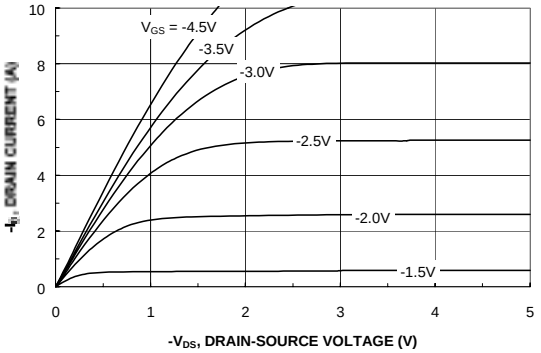


Figure 11. On-Region Characteristics.

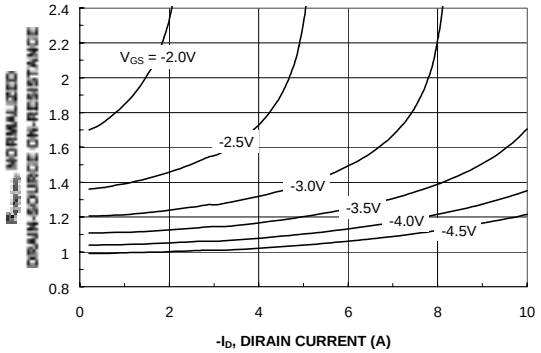


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

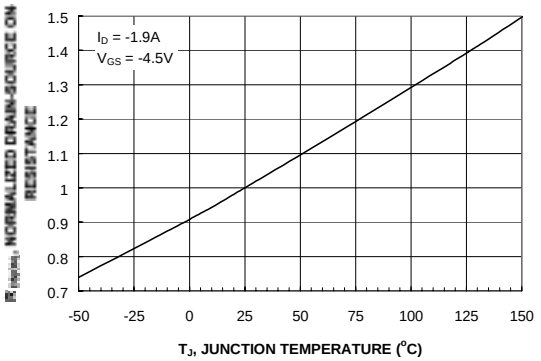


Figure 13. On-Resistance Variation with Temperature.

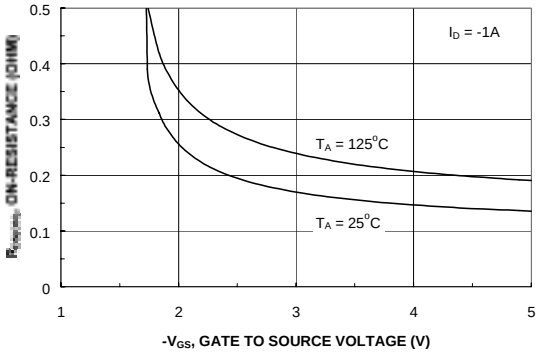


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

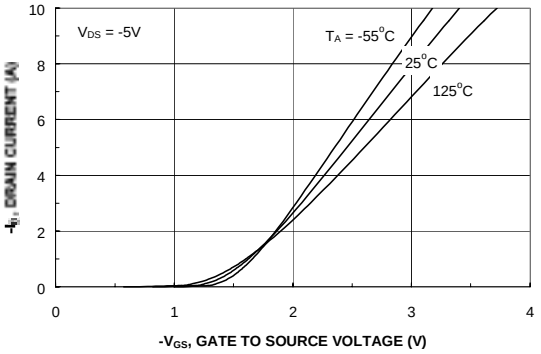


Figure 15. Transfer Characteristics.

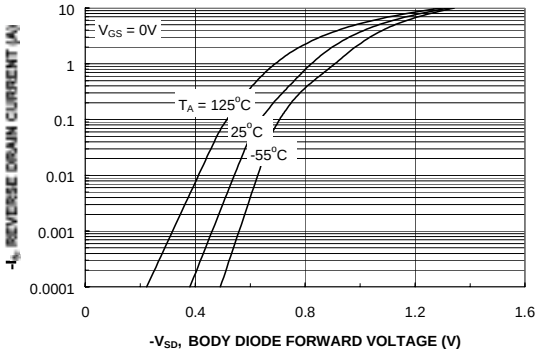


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: P-Channel (continued)

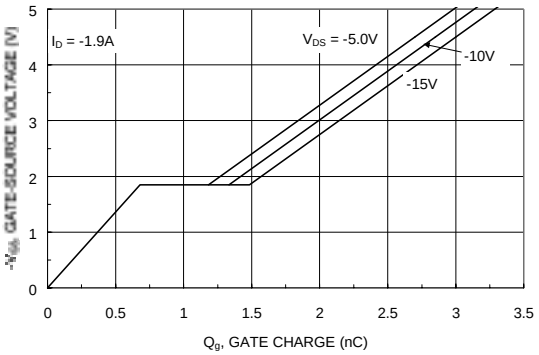


Figure 17. Gate-Charge Characteristics.

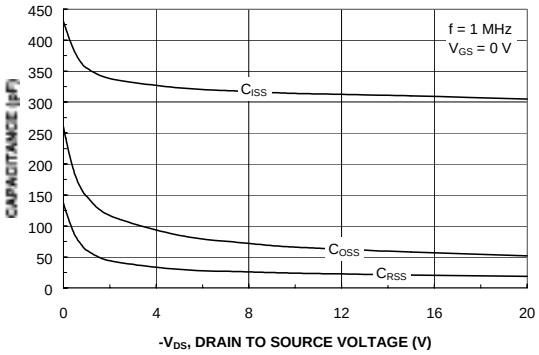


Figure 18. Capacitance Characteristics.

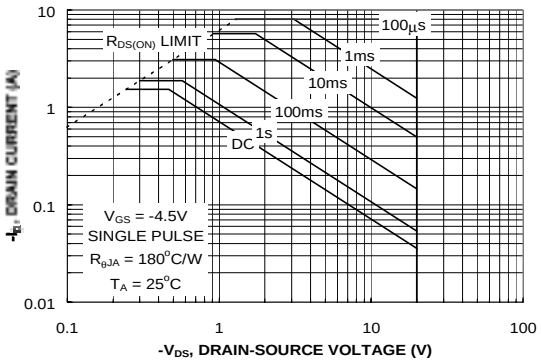


Figure 19. Maximum Safe Operating Area.

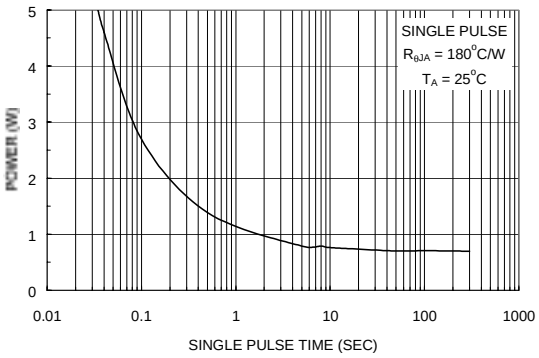


Figure 20. Single Pulse Maximum Power Dissipation.

Typical Characteristics: N & P-Channel (continued)

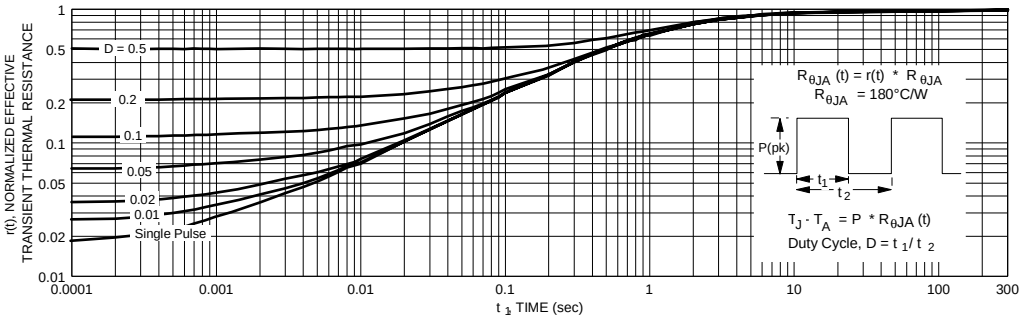


Figure 21. Transient Thermal Response Curve.

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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